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Objective

Computer and Systems Architecture (Design, Implementation, Tool Support, Programming and Programming Models) including General-purpose and Application-specific Architectures and Hardware Accelerators (Numerical and Cryptographic Applications). Focus on Dynamically Reconfigurable and Self-organizing Architectures.

Education

- Technische Universität München, Doctorate Degree (Dr. rer. nat.) *magna cum laude*, December 2002
Doctorate Thesis Title: *Cryptonite – A Programmable Crypto Processor Architecture for High-Bandwidth Applications*
- Technische Universität München, Diploma Degree (Dipl. Inform.; equivalent to M.Sc.) in Computer Science (major) and Electrical Engineering (minor), April 1997
- Wentzinger Gymnasium Freiburg, Abitur (university-entrance diploma), June 1991

Related Job Experience (13 years)

- Senior Research Associate since 01/2004
Universität Karlsruhe (TH), Karlsruhe, Germany

Pursuing previous work on processor architectures, the hardware and system aspects of autonomic and so-called organic or bio-inspired computing are investigated, i.e. if and how parts of the architecture itself can be changed in a running system to adopt to given constraints such as speed, energy consumption, and fault tolerance.

Special focus is put on flexible, runtime-reconfigurable architectures while maintaining binary compatibility among all possible configurations. Example scenarios are numerical accelerator architectures exploiting program phase behavior, and Software-defined radio. For this, a dedicated hardware and software platform was developed to explore runtime reconfigurability using no-overhead dynamic function mapping during program execution. Further work is pursued in the field of Self-Organization including the bio-inspired Digital on-demand Computing Organism for Real-time Systems (DodOrg), and self-organizing memory subsystem called Self-aware Memory (SaM) for heterogeneous, parallel, and dynamically changing architectures.

Further work addresses tools for parallel programming and parallel programming models, where one focus currently lies on implementation and use of Transactional Memory, where we developed GCC-TM, i.e. an STM implementation based on the GCC compiler suite.

DodOrg is funded by the German Research Foundation (DFG).

GCC-TM is a research collaboration with and funded by INRIA Saclay through HiPEAC.

- Consultant: Security Architect and Circuits Design 03/2003–12/2003
Agere Systems, Holmdel, NJ, USA

Development of speed- & area-optimized stand-alone crypto cores for interfacing with or integration into dedicated high-speed network processor architectures and general purpose processor cores.

- Intern: Programmable High-performance Cryptographic Architectures 09/2001–10/2001
Bell Labs Research / Agere Systems, Murray Hill, NJ, USA
 Internship as part of the development of a novel programmable processor architecture dedicated to crypto algorithms. The architecture was created to fulfill the needs of selected crypto algorithms which were implemented on architecture simulators; furthermore, parts of the architecture were realized as VHDL models to determine hardware requirements.
(continued on next page)

- Research Assistant 11/1998-03/2003
Technische Universität München, Munich, Germany
 Research and development work focusing on application-specific, configurable architectures. Work included vertical migration of DSP algorithms into FPGA architectures, and hardware-based translation of Java bytecode into native assembly language of arbitrary microprocessors.
 Industry cooperation with Force Computers GmbH/Solectron (Neubiberg, Germany) targeting fault-tolerant computing, including participation within PICMG standardization work (2.13: Redundant System-Slot Specification; 2.14: Multicomputing Specification). This work was funded by the Bavarian Science Foundation (BFS).
 Further industry cooperations with Infineon Technologies AG (Munich, Germany) on embedded parallel processing and application specific processors such as network and communication processors. In addition, the project covered tools and simulators needed for the simulation of such architectures.

- Field Application Engineer 07/1998-10/1998
Vantis GmbH, Munich, Germany
 Field Application Engineer for Programmable Logic Devices (PLDs, CPLDs) with key account OEM customer responsibility.

- Application Engineer (Trainee/Part-time) 05/1996-06/1998
AMD/Vantis GmbH, Munich, Germany
 Application Engineer for Programmable Logic Devices. Work included participation in the Software Development Group (Design Synthesis); Field Application work including customer design help and fixing.

Additional Experience

- System and Web Administration since 1987
 System Administration in heterogeneous company networks including NIS, NFS, Samba, and Novell Networkware and mixed PC/Unix Workstations running Solaris, Linux, Windows and DOS. Includes administration of public chatrooms and BBS Systems.
 Corporate administration done for AMD GmbH (Munich, Germany; 05/1996-12/1996), Connection Universe GmbH (Munich, Germany; 01/1995-04/1996), Buchty&Häringer Steuerberatungsges.mBh (Freiburg, Germany; 12/1987-08/1991).
 Freelance administration of shared web- and database servers since 1997 for MEMI.de, digitstudios.de, bonsai-multimedia.de, kanzlei-hannak.de, buchty.net, buchty.org, and others.

- Freelance Journalist since 1996
 Editorial staff member of *Go64! – Das Magazin für wahre Computerfans* (CSW Verlag, Winnenden, Germany; 01/1998-09/2001) and *Lotek64* (Fuchs, Vienna, Austria; since 12/2004). Freelance work for *Digital Magazin* (Digital Equipment Corporation, Munich, Germany; 06/1996), *ComputerChannel* (Gruner&Jahr, Hamburg/Munich, Germany; 03/2000-12/2000), *Keys* (PPV Verlag, Holzkirchen, Germany; 08/2000).
 Co-Publisher of *MEMI – Das Magazin für Elektronische Musik im Internet* since 1997.

- Freelance Programmer since 1997
 Web and database development as part of the administration of MEMI.de and others (since 1997). Audio application development (C/C++) for Native Instruments Software Synthesis GmbH, Berlin, Germany (as subcontractor of Nexoft, Munich, Germany; 2002).

Professional Activities

- Reviewer for various international Journals, Conferences, and Workshops
- Organizer, Program, and Technical Committee Member of various international Conferences and Workshops
- Member of the European Network of Excellence (NoE) on High-performance and Embedded Architecture and Compilation (HiPEAC)
- Member of Gesellschaft für Informatik e.V.

Third-party Funding

- “BALANCE”, joint industrial research project with Force Computers GmbH, Neubiberg. Funded by the Bavarian Science Foundation (Bayerische Forschungsförderung, BFS); 2-year project (2003-2005) w/ 2 researcher positions (Contributor)
- HiPEAC Travel Grants to accommodate for cluster meetings and research visits w/ Univ. Edinburgh (2006) (Coordinator and Contributor)
- HiPEAC Travel Grant to accommodate for cluster meetings and research visits w/ TU Delft (2007) (Coordinator and Contributor)
- “DodOrg: Plasticity, Dynamics, and Stability”, interdisciplinary university research project. Funded by the German Science Foundation (Deutsche Forschungsgemeinschaft, DFG); 1-year project (2009) w/ 4 researcher positions (Coordinator and Contributor)
- HiPEAC Collaboration Grant for financing a research visit at TU Delft in 2009 for joint work on a reconfigurable platform (Applicant and Coordinator)
- “DodOrg: Stability and Robustness”, interdisciplinary university research project. Funded by the German Science Foundation (Deutsche Forschungsgemeinschaft, DFG); 2-year project (2009) w/ 4 researcher positions (Coordinator and Contributor)

Activities

Personal interests include reading, creative writing, music composition as well as developing, reverse-engineering, and improving electronic devices w/ focus on electronic musical instruments.

Languages

Human Languages: German (native), English (fluent), French (basic), Latin (basic)

Various programming, hardware design, and further languages including C, C++, SystemC, VHDL, Verilog, Perl, PHP, Python, HTML, JavaScript, \LaTeX , and several assembly languages.

Patents and Patent Applications

- Rainer Buchty, Nevin Heintze, Dino P. Oliva: *Vector Indexed Memory Unit and Method*; U.S. Patent Office Serial Number 7,299,338; granted November 20, 2007 (filed November 25, 2003: 10/722100, published August 5, 2004: US2004/0153623)
- Rainer Buchty, Nevin Heintze, Dino P. Oliva: *Encryption Unit*, U.S. Patent Office Serial Number 60/430749 (provisional patent); filed December 4, 2002; expired August 1, 2004 (benefits claimed by USPTO S/N 10/722100)

Books

- Rainer Buchty, Jan-Philipp Weiß (Editors): *High-performance and Hardware-aware Computing*, Proceedings of the First International Workshop on New Frontiers in High-performance and Hardware-aware Computing (HipHaC'08) held in Conjunction with MICRO-41, ISBN 978-3-86644-298-6, Universitätsverlag Karlsruhe, November 2008

Publications

- David Kramer, Rainer Buchty, Wolfgang Karl: *A Scalable and Decentral Approach to Sustained System Monitoring*, in: Proceedings of the 5th HiPEAC Summerschool on Advanced Computer Architecture and Compilation for Embedded Systems (ACACES), Academia Press, La Mola, Spain, July 2009
- Rainer Buchty, Mario Kicherer, David Kramer, and Wolfgang Karl: *An embrace-and-extend approach to managing the complexity of future heterogeneous systems*, in: Proceedings of Samos IX, Springer, Series Lecture Notes in Computer Science (LNCS) Volume 5657, pp. 226-235, Samos, Greece, July 2009
- Fabian Nowak and Rainer Buchty: *Providing Guidance Information for Application Mapping on Heterogeneous Parallel Systems*, 22nd PARS Workshop, Parsberg, Germany, June 4/5, 2009 to appear in: PARS Newsletter #26, GI/ITG, ISSN 0177-0454, December 2009
- Oliver Mattes, Fabian Nowak, Rainer Buchty, and Wolfgang Karl: *Augmenting the Curriculum targeting Hardware-aware System Design*, Proceedings of CDNLive! EMEA 2009, Munich, May 2009
- Rainer Buchty, David Kramer, Mario Kicherer, Wolfgang Karl: *A Light-weight Approach to Dynamical Run-time Linking Supporting Heterogeneous, Parallel, and Reconfigurable Architectures*, to appear in: Proceedings of the 22st International Conference on Architecture of Computing Systems (ARCS 2009), Springer, Series Lecture Notes in Computer Science (LNCS) Volume 5455, pp. 60-71, Delft, The Netherlands, March 10-13, 2009
- Rainer Buchty, David Kramer, Fabian Nowak, Wolfgang Karl: *A Seamless Virtualization Approach for Transparent Dynamical Function Mapping targeting Heterogeneous and Reconfigurable Systems* to appear in: Proceedings of the Fifth International Workshop on Applied Reconfigurable Computing (ARC 2009), Springer, Series Lecture Notes in Computer Science (LNCS) Volume 5453, pp. 362-367, Karlsruhe, Germany, February 16-18, 2009
- Fabian Nowak, Rainer Buchty, David Kramer, Wolfgang Karl: *Exploiting the HTX-Board as a Coprocessor for Exact Arithmetics*, Second International Workshop on HyperTransport Research and Applications (WHTRA 2009), Mannheim, Germany, February 12, 2009
- David Kramer, Thorsten Vogel, Rainer Buchty, Fabian Nowak, Wolfgang Karl: *A General-purpose HyperTransport-based Application Accelerator Framework*, Second International Workshop on HyperTransport Research and Applications (WHTRA 2009), Mannheim, Germany, February 12, 2009
- Rainer Buchty, Wolfgang Karl: *Design Aspects for Self-Organizing Heterogeneous Multi-Core Architectures*, in: it – Information Technology Journal, Volume 50, Issue 5/08 “Computer Architecture – New Developments”, pp. 293-299, Oldenbourg Wissenschaftsverlag, ISSN 1611-2776, 2008
- Rainer Buchty, David Kramer, Wolfgang Karl: *An Organic Computing Approach to Sustained Real-time Monitoring*, in: “Biologically-Inspired Collaborative Computing (BICC08)”, pp 151-162, Springer, IFIP Vol. 268, ISBN 978-0-387-09654-4, Milan, Italy, September 2008
- Jie Tao, Marcel Kunze, Fabian Nowak, Rainer Buchty, Wolfgang Karl: *Performance Advantage of Reconfigurable Cache Design on Multicore Processor Systems*, in: International Journal of Parallel Programming, Volume 36, Number 3, pp. 347-360, Springer, ISSN 0885-7458 / 1573-7640, June 2008
- Rainer Buchty, Oliver Mattes, Wolfgang Karl: *Self-aware Memory: Managing Distributed Memory in an Autonomous Multi-Master Environment*, in: Proceedings of the 21st International Conference on Architecture of Computing Systems (ARCS 2008), pp 98-116, Springer, Series Lecture Notes in Computer Science (LNCS), Volume 4934, ISBN 978-3-540-78152-3, Dresden, Germany, February 2008
(Best Presentation Award)

- Fabian Nowak, Rainer Buchty, Wolfgang Karl: *Adaptive Cache Infrastructure: Supporting dynamic Program Changes following dynamic Program Behavior*, in: Proceedings of the 9th Workshop on Parallel Systems and Algorithms (PASA 2008), pp 59-68, GI e.V., Series Lecture Notes in Informatics (LNI), Volume 124, ISBN 978-3-88579-218-5, Dresden, Germany, February 2008
(2nd place “Best PASA Junior Researcher Contribution”)
also published in: PARS Newsletter #25, pp. 49-58, GI/ITG, ISSN 0177-0454, December 2008
- Jie Tao, Asadollah Shahbahrami, Ben Juurlink, Rainer Buchty, Wolfgang Karl, Stamatis Vassiliadis: *Optimizing Cache Performance of the Discrete Wavelet Transform Using a Visualization Tool*, in: Proceedings of the 2007 IEEE International Symposium on Multimedia (ISM-07), pp. 153-160, ISBN 978-0-7695-3058-1, Taichung, Taiwan, December 2007
- Rainer Buchty, Fabian Nowak, Wolfgang Karl: *A Run-time Reconfigurable Cache Architecture*, in: Proceedings of the International Conference ParCo 2007, pp. 757-766, IOS Press, Series “Advances in Parallel Computing”, Volume 15, ISBN 978-3-9810843-4-4 (ParCo 2007), Jülich, Germany, September 2007
- Hans-Peter Löb, Rainer Buchty: *A Network Agent for Diagnosis and Analysis of Real-time Ethernet Networks*, in: International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES 2006), pp. 65-73, ACM Press, ISBN 1-59593-543-6, Seoul, Korea, October 2006
- Rainer Buchty, Wolfgang Karl: *A Monitoring Infrastructure for the Digital on-demand Computing Organism (DodOrg)*, in: Self-Organising Systems: First International Workshop, IWSOS2006, p. 258, Springer, ISBN 3-540-37658-5, Passau, Germany, September 2006
- Rainer Buchty, Jie Tao, Wolfgang Karl: *Automatic Data Locality Optimization through Self-Optimization*, in: Self-Organising Systems: First International Workshop, IWSOS2006, pp. 187-201, Springer, ISBN 3-540-37658-5, Passau, Germany, September 2006
- Rainer Buchty, Wolfgang Karl: *The Digital On-demand Computing Organism for Real-time Applications*, ACACES 2006 Poster Abstracts, pp. 41-44, Academia Press, ISBN 90-382-0981-9, L’Aquila, Italy, Juli 2006
- Rainer Buchty: *Reconfigurable Architectures and Instruction Sets: Programmability, Code Generation, and Program Execution*, Dagstuhl Seminar 06141 “Reconfigurable Architectures”, Dagstuhl Castle, Germany, April 2006
- Georg Acher, Rainer Buchty, Carsten Trinitis, *CPU-independent Assembler in an FPGA*, FPL’05 – Proceedings of the 2005 International Conference on Field Programmable Logic and Applications, pp. 519-522, IEEE CS, ISBN 0-7803-9362-7, Tampere, Finland, August 2005
- Rainer Buchty, Georg Acher, Jürgen Jeitner, Wolfgang Karl, Jie Tao, Carsten Trinitis, *ASoCS: An Architecture Concept for Self-optimizing Parallel and Distributed Computer Systems*, PARS’05 Workshop Proceedings, Kiel, Germany, June 2005
also published in: PARS Newsletter #22, pp. 108-117, GI/ITG, ISSN 0177-0454, December 2005
- Rainer Buchty, *Modelling Cryptonite: On the Design of a Programmable High-Performance Crypto Processor*, ARCS 2004 Organic and Pervasive Computing Workshop Proceedings (LNI P-41), pp. 318-327, Gesellschaft für Informatik, ISBN 3-88579-370-9, Frankfurt/Main, Germany, March 2004
also published in: PARS Newsletter #21, pp. 11-20, GI/ITG, ISSN 0177-0454, December 2004
- Rainer Buchty, Nevin Heintze, Dino Oliva, *A Programmable Crypto Processor Architecture for High-Bandwidth Applications*, in: ARCS 2004 International Conference on Architecture of Computing Systems Proceedings (LNCS 2981), pp. 184-197, Springer, ISBN 3-540-21238-8, Frankfurt/Main, Germany, March 2004
- Dino Oliva, Rainer Buchty, Nevin Heintze, *AES and The Cryptonite Crypto Processor*, CASES 2003 Conference Proceedings, pp. 198-209, ACM Press, ISBN 1-58113-676-5, San Jose, CA, USA, October 2003
- Rainer Buchty, *Cryptonite - A Programmable Crypto Processor Architecture for High-Bandwidth Applications*, Doctorate Thesis, Technische Universität München, December 2002